Abdullah Al Sajid

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Research Interests

Hardware Acceleration, Hw/Sw Co-design, Domain-specific Accelerators, HLS, FPGA, ML Edge Deployment, Chip Design

Current Research Focus: Acceleration of CNNs and GNNs on resource-constrained devices.

Open to: exploring hardware acceleration across new domains or deeper specialization within existing areas.

Ongoing Independent Investigations

Adaptive Precision CNN with Dynamic Partial Reconfiguration

Investigating cascaded early-exit strategies for medical edge inference

- Exploring Dynamic Partial Reconfiguration for multi-tier classification
- **Goal:** balancing diagnostic accuracy with power constraints on resource-limited FPGAs
- **Problem Addressed:** Medical AI deployment where false negatives are critical but continuous high-precision inference is energy-prohibitive.

Node-Centric GNN Inference on Resource-Constrained FPGAs

Investigating memory-efficient message-passing for edge deployment

- Exploring node-parallel computation patterns
- **Goal:** reduce memory bandwidth requirements on low-end FPGAs (Zynq-7000 class).
- **Problem Addressed:** GNN inference feasibility on edge devices where traditional matrix-heavy approaches exceed memory/compute budgets.

Education

University of Dhaka 2020-2025

Bachelor of Science in Electrical and Electronics Engineering (Major: Electronics, Minor: Communications) *Dhaka, Bangladesh*

- **Relevant Coursework:** VLSI Design, Digital Electronics with Verilog, Analog Electronics, Microprocessor and Organization, Semiconductor Technology, Quantum Mechanics, Nanotechnology, Electronic Devices

Research

Thesis: DNN Acceleration in Resource-Constrained Devices with FPGA Implementation 2024-2025

Supervisors: Dr. Mosabber Uddin Ahmed & Dr. Sharnali Islam

- **Outcome 1:** Accelerated a reduced VGG-11 CNN, achieving **1900 images/s** throughput. Models deployed with 1-bit and 2-bit quantization with **2% accuracy drop** compared to the FP32 baseline on Pynq-Z2 FPGA
- **Outcome 2:** Designed and implemented a 2-layer Graph Convolutional Network (GCN) with custom Brevitas layers and QAT. Explored FPGA PS deployment through ONNX at various quantization levels.
- **Outcome 3:** Identified key bottlenecks in existing frameworks, with plans for enhancement to include support for networks such as GNN/Transformers.

Research Assistant 2022 – 2023

Bangladesh Computational Social Science Lab (BCS2) *Remote, USA*

- **Broad Contribution 1:** Engineered a multi-threaded Python data processing pipeline, achieving a **7x reduction in processing time** for arxiv, pwc and scopus datasets. Analyzed the ethical compliance and disclosure strategy of firms in AI-ethics research.
- **Broad Contribution 2:** Contributed to multiple projects by conducting literature reviews and developing data visualizations to analyze industry involvement in AI research.

Posters & Presentations

Sajid, A. A., Ahmed, M.U., Islam, S., "FPGA Based CNN Accelerator Design for low-power devices". Poster accepted at the Bangladesh AI, Electronics, and Robotics (BEAR) Summit & National Semiconductor Symposium, Dhaka, Bangladesh. (July, 2025)

Relevant Projects

Object Detection using YOLO-v3 on FPGA

Python, Vivado, PetaLinux, Xilinx DNNDK, C++

- Implemented the quantized **YOLO-v3** model through **DPU** (Deep Learning Processing Unit) for object detection on traffic images
- Configured **PetaLinux** on the ZYNQ PS for management of DPU Inference Engine and post-processing.
- Quantized YOLO-v3 using **Xilinx DNNDK**, optimizing the model for FPGA resource constraints and improved inference time by **6x** compared to CPUs, and similar performance to GPUs while consuming **10x** less power.

Classical Simulation of Quantum Computation

C++, Vitis HLS, Vivado, Python

- Implemented a **single-qubit** classical simulator for Quantum Computing using **HLS**.
- Utilized the AXI-Streaming interface with DMA and HLS optimizations to achieve 5ns latency (HLS Core) and operation time of 0.0361μs (100k simulations). Investigated resource usage and timing constraints on PYNQ-Z2.
- Working on extending the design for multi-qubit, multi-gate simulation to explore entanglement.

CORDIC Algorithm Hardware Accelerator

C++, Vitis HLS, Vivado, Python

- Implemented a **CORDIC (COordinate Rotation DIgital Computer) accelerator** using **High-Level Synthesis** for efficient computation of trigonometric functions.
- Optimized the design with **fixed-point arithmetic, pipelining, and loop unrolling** to achieve nanosecond latency.

Experience

Pristine Crossing Point Ltd. 2025 – present

Project Hardware Engineer *Dhaka, Bangladesh*

- Led the development, design and deployment of an IoT enabled Water Desalination plant for coastal regions of Bangladesh, providing drinking water for over 2000 residents.
- Led the development, design and deployment of IoT enabled Early-Streamer lightning protection systems for coastal regions of Bangladesh, providing safety during thunderstorms for over 50 households.
- Communication with multiple cross-country teams for the design, development and validation of technical infrastructure for various IoT enabled projects in-progress.

Pristine Crossing Point Ltd. 2021 – 2023

Project Officer (Technical) *Dhaka, Bangladesh*

- Worked closely with the Managing Director during the inception phase of the **Solar powered water-filtration system**, among other key projects.
- Performed technical evaluations, international site visits and systems design for deploying renewable systems in remote areas.

Relevant Technical Skills

Languages: C/C++, Python, Verilog, MATLAB, TCL
Frameworks & Libraries:PyTorch, Pytorch-Geometric, Brevitas, ONNX, iVerilog, GTKWAVE
Tools & Platforms: Vivado, Vivado HLS, Vitis, Cadence Virtuoso, OpenLane2, Linux, Blender, PSpice, Git, VirtualBox
Concepts: FPGA Workflow, RTL Design, High-Level Synthesis (HLS), Computer Architecture, Graph data systems, Scheduling, Binding,Neural Networks, Parallel Computing, Image Processing

Leadership and Training

IEEE SIGHT University of Dhaka 2022–2024

Project Technical Member

- Led deployment of two community-driven solutions: **Archer** (low-cost Linux computing) and **beShuddho** (RO/UV water purification).
- Secured **$2500 IEEE funding** and demonstrated leadership in resource management and stakeholder coordination.
- Implemented solutions impacting over 500 individuals in rural communities.

IEEE Student Branch University of Dhaka 2021–2022

Webmaster

- Managed branch websites, implemented subdomains for modular society activities, and enhanced security with plugins and scripts.
- Trained incoming webmasters, conducted sessions, and evaluated member progress.

Relevant Awards

Ulkasemi VLSITHON 2.0 2024

Finalist – RTL & Analog Circuit Design

IEEE EDS Poster Design Competition 2022

Champion – Technical Poster, University of Dhaka